REMARKS

The application was filed on 10 September 1999 with twenty-one claims. The Examiner, on 03 October 2002, first rejected claims 4-7, 17, 16 and 19 under 35 U.S.C. §112; claims 19 and 20 under 35 U.S.C. §102(e) as being anticipated by U.S. Patent 6,385,708 entitled *USING A TIMING-LOOK-UP-TABLE AND PAGE TIMERS TO DETERMINE THE TIME BETWEEN TWO CONSECUTIVE MEMORY ACCESSES* to Stracovsky et al. (Stracovsky '708); and claims 1-21 under 35 U.S.C. §103(a) as being unpatentable over Stracovsky '708 in view of U.S. Patent No. 6,088,772 entitled *METHOD AND APPARATUS FOR IMPROVING SYSTEM PERFORMANCE WHEN REORDERING COMMANDS* to Harriman et al. (Harriman '772). Applicants revised the specification and amended claims 1, 16, 17, and 19 to remove rejections under 35 U.S.C. §112. Applicants traversed the rejection of the claims based on the art of Stracovsky '708 alone and in combination with Harriman '772. Applicants submitted formal drawings. The Examiner finally rejected claims 19 and 20 under Stracovsky '708, and claims 1-18, 21 under Stracovsky '708 and Harriman '772. Applicants attempted to amend the claims to put them in condition for allowance and/or in better condition for appeal but the amendments were not entered.

On 23 July 2003, Applicants filed a Request for Continued Examination. The Examiner then issued a new rejection of claims 19 and 20 under 35 U.S.C. §103(a) over Stracovsky '708 and U.S. Patent No. 6,601,151 entitled Apparatus and *METHOD FOR HANDLING MEMORY ACCESS REQUESTS IN A DATA PROCESSING SYSTEM* to Harris (Harris '151), but still maintained the original rejection of claims 1-18 and 21 under 35 U.S.C. §103(a) over Stracovsky '708 and Harriman '772. Applicants traversed the rejections under 35 U.S.C. §103(a) over the combinations of Stracovsky '708 with Harriman '772 or with Harris '151.

The Examiner then rejected claims 1-18 and 21 under 35 U.S.C. §103(a) as being unpatentable over Stracovsky '708 and Harriman '772 and U.S. Patent No. 6,145,052 entitled *DISK DRIVE WITH ADAPTIVE POOLING FOR COMMAND REORDERING* to Howe et al. (Howe '052); the Examiner also rejected claims 19 and 20 under 35 U.S.C. §103(a) as being unpatentable over Stracovsky '708 and Harris '151 and Howe '052. Claims 19 and 21 are amended. Claims 1-21 are pending.

The Rejection Under 35 U.S.C. § 103(a) over Stracovsky '708, Harriman '772, and Howe '052

The Examiner rejected claims 1-18 and 21 as being obvious in view of Stracovsky '708 and Harriman '772 and Howe '052. Stracovsky '708 proposes a universal controller between multiple processors and multiple devices, e.g., a large memory shared by the multiple processors and/or devices, wherein the controller issues a universal command. The controller further has a circuit designed to specifically avoid data transfer collisions when commands access the same device. When the universal controller is a memory controller accessing a synchronous link dynamic random access memory (SLDRAM), a command is issued to memory only when its command issue time is zero which means that no other events must occur before the command can issue. The value of the command issue time for a particular command indicates the latency between two commands to the same bank and is determined largely by the physical characteristics of the accessed resource, e.g., memory. Given a command with a zero issue time, Stracovsky '708 will not allow another command to issue to the same bank until the first command is issued in order to avoid collisions. Thus, Stracovsky '708 does consider the memory cycle latency of the next command before it issues. The Examiner admits, however, that Stracovsky '708 does not specifically teach placing each received

command into its own command type queue and then reordering the command in each queue so that one categorized command with the least memory cycle performance penalty is selected for execution and then executing sequential valid commands of the same command type. For those features, the Examiner relies on Harriman '772 and Howe '052.

Harriman '772 teaches a memory access controller in which memory commands are first separated into queues depending on the type of command, i.e., a normal priority read queue, a normal priority write queue, and a high priority read and write queue. Only normal priority read commands, *see* column 5, lines 4-7 and column 6, lines 21-23, are reordered first by access to the same memory page number as a previously issued command and then reordered based on age. Normal priority read commands to the same memory portion are fenced and a number of commands are allowed to execute up to a fence count of a number of quadwords. Harriman '772 teaches that it is favorable for sequential commands to access the same portion of memory and does not consider the least memory cycle performance penalty when reordering and grouping normal priority read commands. The Examiner admits that neither Stracovsky '708 nor Harriman '772 teach reordering categorized commands in each of said queues so that one categorized command in each of the queues having the least memory cycle performance penalty is selected for execution; for that aspect of the claims, the Examiner relies on Howe '052.

Howe '052 teaches access to a memory wherein requests to memory are pooled according to the ages of the commands. There is a execution threshold age, a pool threshold age, an age threshold age, and a mechanical time delay. The execution threshold age is predetermined based on, e.g., some time less than a host time-out wherein the host expects a single command to complete, on the order of four to five seconds. The pool threshold age is about half the execution threshold age. The age threshold age may be set to the execution

threshold age less one second. The mechanical time delay is determined based on a seek time from the ending position of the memory cylinder/head at the current command to the starting position of the next command. Quite simply, the commands are considered in order of age, oldest first.

The Examiner thus reasons that it would be obvious "to modify the system of Stracovsky '708 to include placing each received command into a queue pertaining to its respective command type and executing sequential valid commands of the same command type because it was well known to benefit by provide an adequate command reordering mechanism which balances latency and bandwidth concerns while optimizing based on performance criteria such as locality and/or command type as taught by Harriman '772; and to include reordering categorized commands in each of the queues so that one categorized command in each of said queues having the least memory cycle performance penalty is selected for execution because it was well know to beneficially ensure that commands received are efficiently completed within a given time period thus improving system performance as taught by Howe '052."

Applicants respectfully traverse the rejection under 35 U.S.C. §103(a) under the alleged combination of Stracovsky '708, Harriman '772, and Howe '052. First, no reference teaches or suggests the language of "reordering said categorized commands in **each of said queues so that one categorized command in each of said queues** having the least memory cycle performance penalty is selected for execution" (claim 1) and "reordering said categorized commands" (claim 17) and "means to compare said memory commands with each of said types with other memory commands/with a current chosen memory command/with a previously chosen memory command of **each of the same types** (claim 21). Harriman '772 is the only reference that reorders commands and the only commands that Harriman '772 reorders are normal priority read commands and Harriman '772 reorders to access the same

memory page, i.e. of achieving overall locality. Applicants, on the other hand, reorder every command type in every queue for the purpose of, *inter alia*, avoiding thrashing. Because no reference teaches or suggests the claimed language, it is impossible for their combination to do so.

Second, another reason the Examiner fails to present a prima facie case of obviousness is that the law clearly requires that the references themselves provide the suggestion for their combination, not the Examiner who has the benefit of hindsight and Applicants' teachings. The suggestion and motivation provided by the references for their combination, moreover, must be specific and cannot be "pie-in-the-sky" desires such as achieving a better product. Such noble purposes as to "increase memory access efficiency," "improve overall locality," and "balance latency and bandwidth" are too generic and do not create a prima facie case of obviousness. Everyone in the field of accessing memory wants to increase memory access efficiency; merely stating an over-broad objective does not create a legally substantive basis of obviousness under 35 U.S.C. §103(a) for an alleged combination.

A third reason the Examiner fails to sustain prima facie obviousness is that the methods and categorization proffered by the references to achieve these standard objectives are contradictory. Neither Stracovsky '708 nor Howe '052 improve overall locality; Stracovsky '708 specifically teaches against accessing memory within the same locality in order to avoid collisions; Howe '052 teaches that overall locality is the least important factor to consider and that it is more important to consider the various ages of the commands. The contradiction between Stracovsky '708 and Harriman '772 has been pointed out to the Examiner and still holds: Harriman '772 teaches a method to access a same portion of memory for time determined by a fence count of quadwords whereas Stracovsky '708 prohibits commands to the same bank from issuing order to avoid data transfer collisions.

Let's see: Harriman '772 separates commands into different queues and reorders only normal priority read commands so that they can access the same memory bank, but applying these teachings to Stracovsky '708 would destroy the purpose of Stracovsky '708 to avoid collisions. Applying Howe '052 which executes the oldest commands first, i.e., commands at or exceeding the execution threshold age, then the pool threshold age, then the age threshold age would destroy the purpose of Harriman '772 to execute the same commands within the fence that access the same memory page. Quite frankly, Attorney for Applicants is quite perplexed at coming to any sort of cohesive combination of the references as posed by the Examiner. And so, Applicants respectfully request the Examiner to withdraw the rejection of claims 1-18 and 21 based on the combination of Stracovsky '708, Harriman '772, and Howe '052.

The Rejection Under 35 U.S.C. § 103(a) over Stracovsky '708, Harris '151, and Howe '052

The Examiner rejected claims 19 and 20 under 35 U.S.C. §103(a) under the combination of Stracovsky '708, Harris '151, and Howe '052. The Examiner asserts that Stracovsky '708 teaches all the claimed elements except for a plurality of comparison logic circuits, each associated with one of a plurality of command FIFO queues. The Examiner reasons that system efficiency would be improved by providing separate queues and associated logic blocks for reads and writes so that the logic blocks can be tailored specifically to the memory access request type, per Harris '151.

Stracovsky '708 is described above with respect to the earlier rejection. Harris '151 teaches a memory controller to increase the throughput of memory access requests in a data processing system independent of memory access times and memory bandwidth. The combination of Stracovsky '708 with Harris

'151 is a combination that achieves the same result: avoidance of data collision. The comparison logic of Harris '151 is not to determine which memory commands have the least memory cycle performance penalty, as in claim 19; the comparison logic of Harris '151 is an address dependency check, indicated to be separate from the memory cycle performance penalty. Howe '052, moreover, does not provide the teaching for comparing memory cycle performance penalties to determine which command issues first; as discussed earlier. Howe '052 ensures that oldest commands are issued. Howe '052 does consider a mechanical time delay but only after the age of the command is determined. In other words, the memory cycle performance penalty of Howe '052 is not determined by comparison of a number of oldest received categorized commands with each other, with a currently chosen command, and with a previously chosen command (amended claim 19); the mechanical time delay is based only on the current command and the next command. Again, respectfully, address dependency among commands and comparison of the ages of the commands are not the same thing as comparison of memory cycle performance penalties as claimed.

Applicants request the Examiner to reconsider and withdraw the rejection of claims 19 and 20 under Stracovsky '708, Harris '151, and Howe '052.

Conclusion

Applicants maintain that Stracovsky '708 and Harriman '772 cannot be combined and their combination would undermine a fundamental objective of each of the references. Stracovsky '708 teaches to avoid accessing the same page of memory while Harriman '772 discloses a method and apparatus to reorder normal priority reads to access data in the same memory bank. Howe '052 simply teaches pooling commands by their ages to ensure that the oldest

commands execute. No single reference teaches that all command types are reordered and the reordering is based on memory cycle performance penalties. Stracovsky '708 nor Howe '052 are concerned with command type. Harriman '772 is concerned only with normal priority reads.

Applicants thus respectfully request the Examiner to reconsider the application in view the amendments and the remarks, and pass the application to issuance. The Examiner is further invited to telephone the Attorney listed below if he thinks it would expedite the prosecution and the issuance of the patent.

Respectfully submitted,
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